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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
PETRANEK, JACOB ANDREW	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 08/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/928,011	SEDLAK ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3 and 4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3 and 4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 3-4 are pending.

2. The office acknowledges the following papers:

Arguments filed 8/2/2006.

Drawings

3. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because figure 3 is missing the selector parameter to the MUX that selects between the two inputs. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d).

Withdrawn objections and rejections:

4. The 35 USC § 112 first paragraph rejections for claims 3 and 4 have been withdrawn.

Maintained Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Goetz (U.S. 5,854,913), in view of Yoshida (U.S. 5,088,030), in view of Mano et al. ("Logic and Computer Design Fundamentals"), in view of May et al. ("The PowerPC Architecture"), and in view of K. Short ("Embedded Microprocessor Systems Design").

7. As per claim 3:

Goetz discloses a microprocessor for processing various assembler codes, comprising:

- Depending on how the parameter is set, a different relative addressing takes place: (Relative addressing is defined as, "An addressing mode in which the effective address is formed by adding an offset to the program counter (or a portion thereof) during execution." (The Authoritative Dictionary of IEEE Standards Terms) Therefore, incrementing a program counter is relative

addressing, because the program counter has a current value, and a new value is reached by adding an instruction length to the current PC address. Since the Q-bit indicates different instruction lengths to be added to the current PC address, different relative addressing takes place dependent on the Q-bit (Figure 9, Column 16, lines 47-64). Column

- A program counter (NIFA Compute 807, figure 9 and column 16, lines 47-64)

- A computation unit for computing relative addresses: (NIFA Compute 807, figure 9 and column16, lines 47-64)

While Goetz teaches multiple instruction sets being implemented and indicated by a parameter, Goetz is silent on how the different offsets for branch instructions are handled. It is well known in the art that PowerPC branch instructions add an offset to the address of the branch instruction (Page 36, numeral 1, The PowerPC Architecture), while x86 branch instructions add an offset to the address of the instruction following the branch instruction (Short, Embedded Microprocessor Systems Design, page 190, 2nd paragraph). However, since Goetz is silent on how the above issue is resolved, Goetz fails to teach:

- A multiplexer having a first input a second input for receiving a zero value, a third input receiving a parameter designating a respective assembler code, a memory for storing an instruction length having an output connected to said first input of said multiplexer

- An addition unit connected between said program counter and said computation unit, said adding unit having a first input connected to said program counter, a

second input for an instruction length, and an output connected to said computation unit:

Yoshida teaches hardware to implement an x86-like branch instruction, which adds an offset to the address of the instruction following the branch instruction:

- A program counter (register 13, figure 2; Column 4, lines 8-20)

- A computation unit for computing relative addresses: (2nd Adder 17, figure 2 and column 4, lines 1-20)

- An addition unit connected between said program counter and said computation unit: (1st Adder 15)

-Said adding unit having a first input connected to said program counter, a second input for an instruction length, and an output connected to said computation unit: (Figure 2, the 1st adder 15 has the program counter (register 13) as an input, has an input for an instruction length ("Word Length"), and has an output connected to said computation unit (2nd Adder 17).

Yoshida teaches that the branch offset is calculated by adding an offset to the address of the instruction following the branch instruction. This occurs by adding a "Word Length" that is part of the instruction decoded (Figure 2 and column 4, lines 1-20)

It would have been obvious to add the hardware of Yoshida to implement the branch target address computation because hardware is inherently necessary in order to carry out the x86 relative branch instructions and because the invention of Yoshida eliminates time required by conventional processors to do branch target calculations (Abstract).

While Goetz, in view of Yoshida, teaches a method for handling the x86 branch instruction, it is still necessary to have hardware to implement the PowerPC branch instruction. One of ordinary skill in the art would have recognized that since the purpose of the 1st adder of Yoshida is to add the appropriate length of the branch instruction in order to complete the branch instruction that adds an offset to the address of the instruction following the branch instruction, in order to appropriately execute PowerPC branch instructions, it would be necessary to add a zero as the "word length" to properly calculate the branch target address. Adding a value other than zero as the "word length" while executing PowerPC branch instructions would result in an incorrect branch target address being calculated. Therefore, it would have been inherent to use a zero input as a word length in the system of Goetz, in view of Yoshida, while executing PowerPC-like branch instructions and to use the appropriate, non-zero value word length when executing the x86-like branch instructions.

However, Goetz in view of Yoshida fails to teach that the "Word Length" values, zero and non-zero values, are stored in a memory and selected via a multiplexer with said parameter as an input.

Since Goetz already teaches a parameter indicating which instruction set's offset to add to the program counter for sequential instruction fetching, one of ordinary skill in the art would have recognized to use the same parameter to indicate which offset to add for different non-sequential instruction fetching, i.e., the branch instructions of each instruction set, in order to avoid redundant hardware.

Furthermore, since the combination of Goetz and Yoshida presents a system in which two instruction sets with two respective branch target address generation schemes are implemented, and in which a Q-bit (Goetz) is already used to indicate which instruction set addressing mode is to be used for a particular instruction, and no hardware implementation has been provided by Yoshida to describe how the "word length" value is generated, one of ordinary skill in the art would have recognized to use a multiplexor to select which one of the two "word length" value types is needed (zero or variable) to present using the Q-bit as the selecting parameter. To further clarify, the combination of Goetz and Yoshida presents a problem of needing to select between two different values for the "word length", one being a zero for PowerPC-like branch instructions, and the other being the normal "word length" used for the x86-like branch instructions. One of ordinary skill in the art would have recognized that a multiplexers function is to select between two options using a controlling parameter (as evidenced by Section 3-7 of Logic and Computer Design Fundamentals, Kime), and since Goetz already teaches the Q-bit being used to indicate to hardware throughout the system which instruction set is currently being executed (x86 or PowerPC), it would have been obvious to use the Q-bit as the selecting parameter input to the multiplexer. Using the multiplexer would provide the advantage of solving the inherent problem of providing the correct "word length" to the 1st adder in figure 2, either a zero or the "word length" that would otherwise be provided when not executing PowerPC-like branch instructions.

8. As per claim 4:

Goetz, Yoshida, Mano, May, and Short fail to teach the only limitation different from claim 3, which is "a subtracting unit" instead of an "adding unit."

However, Examiner takes Official Notice that numbers, including offsets, are very frequently represented in two's complement form, which allows simplified binary arithmetic operations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to have the offsets represented in two's complement form since Examiner takes Official Notice two's complement form allows simplified binary arithmetic operations.

It is inherent that a binary adder is also a subtraction unit if the binary inputs are in two's complement form, because there is no difference in hardware between adding two's complement numbers and subtracting two's complement numbers. A two's complement adder is inherently a subtraction unit as well.

Response to Arguments

9. The arguments presented by Applicant in the response, received on 8/2/2006 are not considered persuasive.

10. The 35 USC § 112 first paragraph rejections for claims 3 and 4 have been withdrawn. Thus, all arguments directed towards these rejections are now moot.

11. Applicant argues "Confusion was added to the non-final rejection mailed on 5/2/2006 from the previous examiner incorrectly labeled the patent Yoshida 4,926,323. This patent number is instead Baror, while U.S. 5,088,030 is for Yoshida. As a result of

the erroneous naming of references in the instant office action, the next office action shouldn't be final."

This argument is not found to be persuasive for the following reason. The name of the inventor was correct, however the patent number used was a typographical error. The previous examiner previously cited Yoshida (U.S. 5,088,030) in the notice of references cited on 1/13/2005. The applicant stated that for the purposes of the instant examination, the applicant would assume that 5,088,030 is the correct patent number that should have been cited in the rejection. This is a correct assumption by the applicant and upon a closer look between the two patents, would have been instantly obvious for the following reasons.

The examiner when picking up this case was also confused by this citation of Yoshida with the wrong patent number. When trying to make a determination if the Baror or the Yoshida reference was intended, the examiner looked at the previous notice of references cited and found a single Yoshida reference being U.S. 5,088,030. Upon looking at these two references, the previous examiner cited in the previous office action sent out on 5/2/2006 for claim 3 that a computation unit and an addition unit were read by a first and second adder in figure 2. Upon looking at figure 2 for both Baror (U.S. 4,926,323) and Yoshida (U.S. 5,088,030), it was immediately obvious that Yoshida (U.S. 5,088,030) was the intended patent used in the rejection. The examiner cites that this process took less than 5 minutes when the mistake was found and doesn't believe it's enough to warrant sending out a non-final rejection because of it.

12. Applicant argues "Confusion was added for claim 4 stating the only difference between claims 3 and 4, which wasn't taught by Goetz, Yoshida, and Baror."

Again, this is a typographical error by the previous examiner and is intended to state that Goetz, Yoshida, Mano, May, and Short fail to teach the single limitation.

13. Applicant argues "Goetz, Yoshida, Mano, May, and Short failed to teach a MUX having a first input, a second input, and a third input to select between the first two."

This argument is not found to be persuasive for the following reason. A multiplexer is well known to one of ordinary skill in the art as having a number of inputs and the necessary number of selector bits. Goetz disclose a processor with two ISA's that can execute on it, which shows in figure 9 that a Power PC and an x86 instruction set could be used. May disclosed a PowerPC architecture, and is used to state that branch instruction target addresses are calculated by adding the branch instruction address and the displacement to calculate the relative address. Short disclosed a x86 architecture, and is used to state that branch instruction target addresses are calculated by adding the instruction length, the PC, and the displacement together to get the relative address. Yoshida disclosed calculating branch instruction addresses for a x86 instruction.

In order to calculate a branch target address for a PowerPC instruction, the instruction length would have to be disregarded and the PC directly added with the displacement. Thus, a selection would have to be made by the processor of Goetz to add the instruction length for a x86 branch or disregard it for a PowerPC branch. It would have been obvious to one of ordinary skill in the art that a MUX could be used to

make this selection, as a MUX is a well-known logic device for selecting between multiple values. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention that a MUX could be added to the combination of Goetz and Yoshida to select the instruction length for x86 branch instructions and select zero for PowerPC branch instructions, with the selecting being done based on which type of branch instruction is occurring for calculating branch instruction target addresses.

14. Applicant states "If the examiner disagrees, a advice on patentable language would be appreciated."

The examiner is unsure what type of amendments would be able to overcome the current claim rejections. It seems that most of the details within specification has at one point or another been included within the claims, with some limitation previously cancelled.

Conclusion

THIS ACTION IS MADE FINAL.

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jacob Petranek
Examiner
Art Unit 2183

EDDIE CHAN
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